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Vertically aligned carbon nanotube field-effect transistors

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ABSTRACT

Vertically aligned carbon nanotube field-effect transistors (CNTFETs) have been developed using pure semiconducting carbon nanotubes. The source and drain were vertically stacked, separated by a dielectric, and the carbon nanotubes were placed on the sidewall of the stack to bridge the source and drain. Both the effective gate dielectric and gate electrode were normal to the substrate surface. The channel length is determined by the dielectric thickness between source and drain electrodes, making it easier to fabricate sub-micrometer transistors without using time-consuming electron beam lithography. The transistor area is much smaller than the planar CNTFET due to the vertical arrangement of source and drain and the reduced channel area.

1. Introduction

The first carbon nanotube field-effect transistor (CNTFET) was reported in 1998 [1] using a semiconducting carbon nanotube as a channel and silicon substrate as a bottom gate. Although the transistor was in its preliminary stage, it represented an important step towards single molecular electronics. Since then, the CNTFETs have been extensively studied because carbon nanotubes have many outstanding mechanical and electrical properties and are expected to supplant silicon in the next generation of field effect transistors [2]. Up to now, CNTFETs have shown excellent performance in the aspects of current ON/OFF ratio [3,4], mobility [5], subthreshod slop [6–8], transconductance [4], and cutoff frequency [9,10]. All these optimizing properties have primarily been achieved on planar transistors with either a bottom gate or a top gate. In comparison, the vertically aligned CNTFETs, to our knowledge, have been rarely studied [11,12], especially for network CNTFETs. Choi et al. [11] have shown vertically aligned CNTFETs using multi-walled carbon nanotubes (MWCNTs), but the gate was isolated from the MWCNT by a dielectric layer and a drain electrode which could screen the gate electric field. Neither the transistor configuration nor the MWCNT material is ideal for a good field-effect transistor (FET). While in Franklin et al.'s report [12], only two terminal devices have been exhibited using single-walled carbon nanotubes (SWCNTs).

Here we present a vertically aligned CNTFET in which source and drain are vertically stacked. Compared with planar transistors, it has two obvious advantages. First, the channel is normal to the substrate surface and the channel length is determined by the thickness of the dielectric layer between source and drain electrodes. In this way, it is easier to fabricate short channel CNTFETs with channel length less than 1 μ using the ordinary lithography. Normally, such a small feature is fabricated using some techniques with high cost and low throughput, for example, electron beam lithography. Second, this FET design requires less space than planar ones, resulting in large integration intensity [13]. It is much important for some special applications in which the transistor area is critical for performance, such as active-matrix organic light-emitting diode (AMOLED) drivers in planar-panel display. The aperture ratio of the AMOLED pixel can be significantly increased by decreasing the transistor area.

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2. Experimental

The transistor configuration used in this study is schematically illustrated in Fig. 1. Different from the planar CNTFETs, source and drain of the transistor are vertically stacked here and they are isolated by a layer of SiN_x. Carbon nanotubes are placed on the sidewall of the stack. It should be noted that the source electrode in the bottom of the stack is purposely made thick. This enhanced source is designed to avoid losing gate control for the SWCNTs near the source electrode. If the stacked bottom source electrode is not high enough, the gate dielectric layer deposited on the protruded source electrode may cause the bottom part of the vertical gate electrode (point A) to be higher than the top part (point B) of the source electrode, leading to weak gate modulation of the SWCNTs in this region.

The fabrication procedure is as follows. First, the source contact composed of 20 nm-Ti and 80 nm-Au was formed using electron beam evaporation (Denton, base pressure 4×10^{-6}Torr) and lithography. Then, the enhanced source, SiN_x and drain were fabricated successively. The enhanced source was 200 nm-Au and 80 nm-Ti. The top Ti (80 nm) layer was used to increase the adhesion between Au and followed 650 nm-SiN_x layer. SiN_x was deposited using a RF sputter at room temperature. The deposition power, target to substrate distance were 100 W, 20 cm, respectively. The drain layer was of 20 nm-Ti and 85 nm-Au.

Commercial SWCNT solution (Nanointegris, IsoNanotubes-STM, semiconductor purity 99%) was used in our experiment. To deposit the SWCNTs on the sidewall of the transistors, some SWCNT solution (10 mg/L in water) were dropped on the Si wafer to cover the entire surface of the active region. The wafer was then placed on a hot plate (150 °C) to evaporate the solvent and leave the SWCNTs on the substrate. Fig. 2 shows the SEM image of the SWCNTs on the sidewall of the stack of enhanced source/SiN_x/drain. Before gate dielectric deposition, the SWCNTs on the outside of the transistor channels were etched using reactive ion etching to isolate the CNTFETs from each other. The power, pressure, oxygen flow and etch time were 150 W, 50 m Torr, 30 sccm and 1 min, respectively.

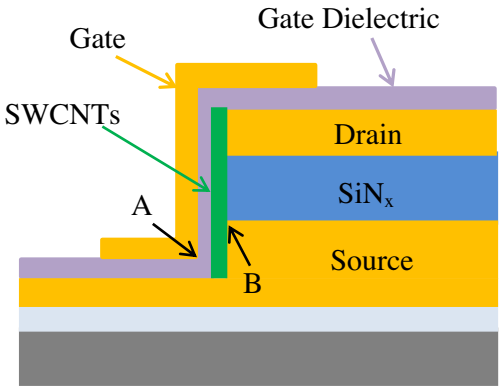

Fig. 1 – Schematic cross section of a vertically aligned CNTFET.

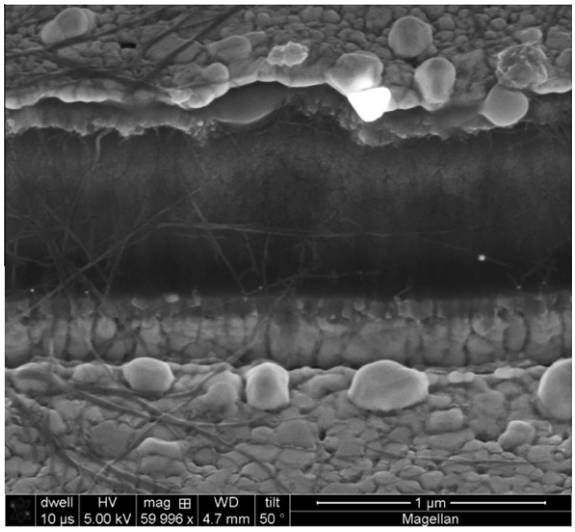

Fig. 2 – SEM image of the SWCNTs on the sidewall of the vertical stack of the CNTFET.

The gate dielectrics were of two layers of HfO_2. In the first step, 80 nm of HfO_2 was deposited by electron-beam evaporation. This layer protected the SWCNTs from being etched by ozone used in the subsequent deposition. After evaporation, the sample was transferred into the atomic layer deposition (ALD) chamber immediately for the deposition of the second layer HfO_2 which was used as high quality, pin-hole-free gate dielectric. The ALD HfO_2 (30 nm) was deposited at 200 °C using a commercial ALD system (Cambridge Nanotech, Savannah100). The precursor, Tetrakis(Dimethylamido)Hafnium and ozone were used in the deposition.

Finally, the whole procedure was completed by depositing the gate layer, 90 nm-Ti and 70 nm-Au, using electron-beam evaporation. Fig. 3 shows a SEM image of the cross section of a typical CNTFET.

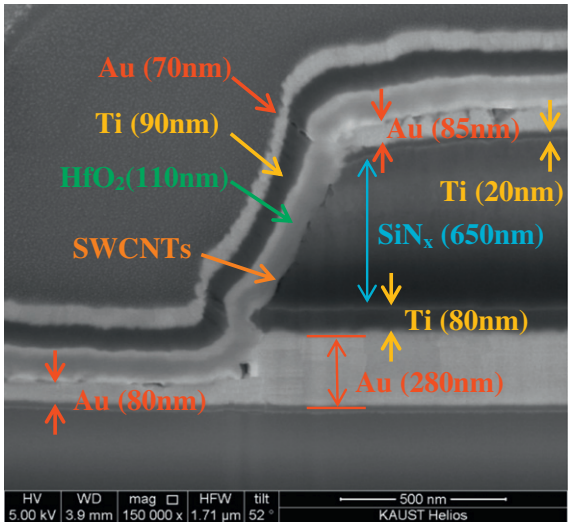

Fig. 3 – SEM image of the cross section of the vertically aligned CNTFET.

3. Results and discussion

The properties of the SWCNTs were analyzed by Raman spectroscopy which was measured using a 473 nm laser. The result is shown in Fig. 4. The large ratio of G^+ (high-frequency component around 1594 cm^{-1}) to G^- (low-frequency component around 1572 cm^{-1}) and the apparent radial breathing mode (RBM) peak at 179 cm^{-1} suggest that the SWCNTs are dominated by semiconducting SWCNTs [14–16]. From the relationship [16] between the diameter of the SWCNT, d, and the RBM frequency, ω,

$$\omega = \frac{234}{d} + 10 \quad (1)$$

we get that the diameter of the SWCNTs is 1.4 nm.

The transfer characteristics of a typical CNTFET are shown in Fig. 5. The black and red curves represent forward (−5 to 5 V) and reverse (5 to −5 V) sweeps of gate voltages, respectively. It can be seen that the transistor exhibits an apparent ambipolar characteristic. The current decreases first with increasing gate voltage and reaches a minimum point at $V_g = -1$ V for forward sweep, then it increases with increasing gate voltage. Normally the CNTFETs with Ti/Au electrodes show p-type characteristics at air environment due to the absorbed oxygen on the metal surface [17,18]. Oxygen plays a role in modifying the work function of the electrodes [17,18], and makes the Fermi level of the electrode lie close to the valance band of the SWCNT. The ambipolar characteristics shown here is because the oxygen adsorbed between electrode and SWCNTs have been removed in high vacuum during the HfO_2 deposition in e-beam evaporation chamber. As a result, the work function of the electrode lies close to the mid-gap of the SWCNTs. The Schottky barriers for electrons and holes are equal, and electrons and holes are injected into the SWCNTs under positive and negative gate voltages, respectively, leading to the ambipolar characteristics.

Fig. 5 also shows obvious hysteresis between forward and reverse sweeps of gate voltage. The hysteresis gap, defined as the difference of threshold voltage between forward and reverse sweeps, is about 3 V, indicating that there are charge injection from carbon nanotubes to their surrounding HfO_2.

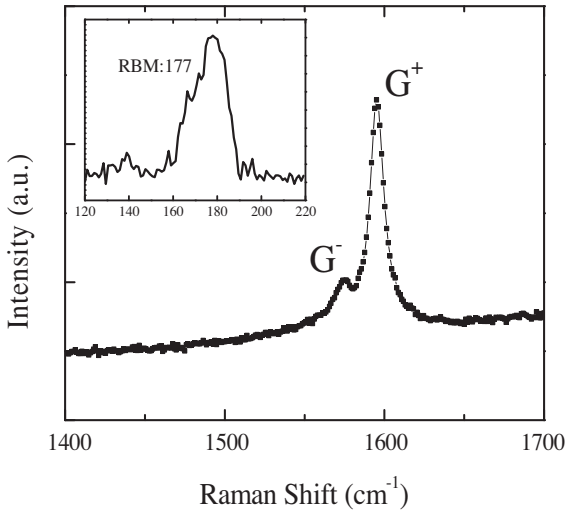

Fig. 4 – Raman spectra of the SWCNTs. Inset: RBM peak of the SWCNTs.

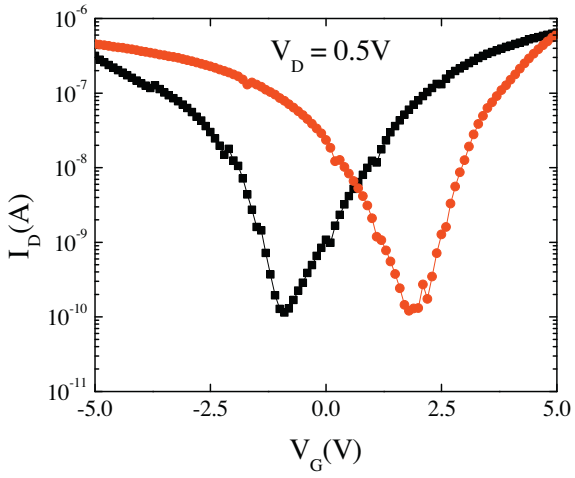

Fig. 5 – Typical transfer characteristics of a vertically aligned CNTFET with V_D = 0.5 V. The black and red curves represent forward and reverse sweeps of gate voltage, respectively. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

The inverse sub-threshold slope

$$S = dV_g/d(\log I_d) \quad (2)$$

is a measure of the switching speed of a transistor. From Fig. 5, we obtain a S value of 350 mV/dec. It is well consistent with the trends of S as a function of the ratio of the effective dielectric constant to the dielectric thickness [19].

The mobility is calculated using

$$\mu = \frac{dI_d}{dV_g} \times \frac{L}{C \times W \times V_d} \quad (3)$$

where L and W are the channel length and width, respectively. C is the capacitance per unit area between the gate and the nanotube network. To take into consideration of electrostatic coupling between carbon nanotubes, the capacitance is expressed as [20,21]

$$C = \left\{ \frac{1}{2\pi\varepsilon_{ox}\varepsilon_0} \ln\left[\frac{2\Lambda_0}{d} \frac{\sinh(2\pi t_{ox}/\Lambda_0)}{\pi} + C_Q^{-1} \right] \right\}^{-1} \Lambda_0^{-1} \quad (4)$$

where t_{ox}, Λ_0^{-1}, and C_Q are gate dielectric thickness, carbon nanotube density and quantum capacitance [22], respectively. Using L = 650 nm, W = 5 μm, $C_Q = 4 \times 10^{-10}$ F/cm^2 [22], d = 1.4 nm, t_{ox} = 110 nm and ε_{ox} = 14 for mixed HfO_2, we calculate the mobility of our 5 CNTFETs. The result is shown in Table 1. The mobility is in the lower range of the reported values (1–90 $cm^2\,V^{-1}\,s^{-1}$) [23] which were obtained from the planar CNTFETs using the same SWCNT source.

The main reason for the low mobility is the low SWCNT density in our CNTFETs. As we know, the mobility of network or thin film CNTFETs depends, to a large extent, on the density of the SWCNTs if we calculate the mobility using the standard method for silicon metal–oxide-semiconductor field-effect transistors. The larger the density is, the larger the mobility is [23–25]. Good alignment of SWCNTs along the channel can improve the mobility further. The largest mobility for solution processed CNTFETs has been reported

Table 1 – Characteristics of five CNTFETs with the same device dimension and different SWCNT density.

CNTFET	SWCNT density (Tubes/μm)	Transconductance (μS)	Mobility ($cm^2 V^{-1} s^{-1}$)
1	1	0.30	5.84
2	2	0.07	0.71
3	2	0.12	1.21
4	3	0.25	1.78
5	4	0.34	1.93

by using high density, well aligned and length-sorted semiconducting SWCNTs [26]. Another reason for the low mobility is the short channel used here. It has been found that the mobility is inversely proportional to the channel length for network CNTFETs [23]. Taking into consideration of low SWCNT density and short channel in our CNTFETs, our result is reasonable.

For short-channel network CNTFETs, Michael et al. [27] reported low ON/OFF ratio (<10) and high ON current (10^{-5} to 10^{-4} A) with channel length of 0.5 μm and channel width of 10 μm. The SWCNTs in their CNTFETs were well aligned and the density is high (10–20/μm). On the contrary, our CNTFETs are fabricated using randomly oriented SWCNTs with low density. The ON current is lower, but the ON/OFF ratio is higher than their results.

4. Conclusion

Vertically aligned CNTFETs have been fabricated using pure semiconducting SWCNTs. The mobility of the CNTFETs is in the lower range of the reported values of the planar CNTFETs using the same SWCNT source, but the advantages of the vertically aligned CNTFETs in short channel fabrication and in transistor area reduction could make them more practical in applications.

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